



Issued Date: May. 30, 2007  
Model No.: M190E5-L0E

**Approval**

## **TFT LCD Approval Specification**

### **MODEL NO.: M190E5-L0E**

Customer: \_\_\_\_\_ BenQ

Approved by: \_\_\_\_\_

Note:

記錄	工作	審核	角色	投票
2007-06-05 12:41:49 CST	Approve by Dept. Mgr.(QA RA)	yuan_chan(趙俊淵 /52760/54760)	Department Manager(QA RA)	Accept
2007-05-31 15:51:48 CST	Approve by Director	davis_wang(王銘典 /56600/54383)	Director	Accept
2007-05-31 14:33:13 CST	Approve by Director	cc_chen(陳春成 /56350/54951)	Director	Accept
2007-05-31 10:52:06 CST	Approve by Director	ck_wei(韋忠光/44700)	Director	Accept



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### REVISION HISTORY

Version	Date	Section	Description
Ver. 3.0	May, 30, 07'	All	M190E5 -L0E Specifications was first issued.



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## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

M190E5-L0E is an 19.0" TFT Liquid Crystal Display module with 4 CCFL Backlight unit and 30 pins 2ch-LVDS interface. This module supports 1280 x 1024 SXGA mode and can display 16.7M colors. The inverter module for Backlight is not built in.

### 1.2 FEATURES

- Wide viewing angle.
- High contrast ratio
- Super fast response time
- High color saturation
- SXGA (1280 x 1024 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- RoHS Compliance

### 1.3 APPLICATION

- TFT LCD Monitor

### 1.4 GENERAL SPECIFICATIONS

Item	Specification			Unit	Note
Active Area	376.32 (H) x 301.056 (V)	(19.0" diagonal)		mm	(1)
Bezel Opening Area	380.2(H) x 305(V)			mm	
Driver Element	a-si TFT active matrix			-	-
Pixel Number	1280 x R.G.B. x 1024			pixel	-
Pixel Pitch	0.294 (H) x 0.294 (V)			mm	-
Pixel Arrangement	RGB vertical stripe			-	-
Display Colors	16.7M			color	-
Transmissive Mode	Normally White			-	-
Surface Treatment	Hard coating (3H), Anti-glare (Haze 25)			-	-

### 1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	395.5	396.0	mm	(1)
	Vertical(V)	323.5	324.0	mm	
	Depth(D)	17.0	17.5	mm	
Weight	-		2100	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.



## 2. ABSOLUTE MAXIMUM RATINGS

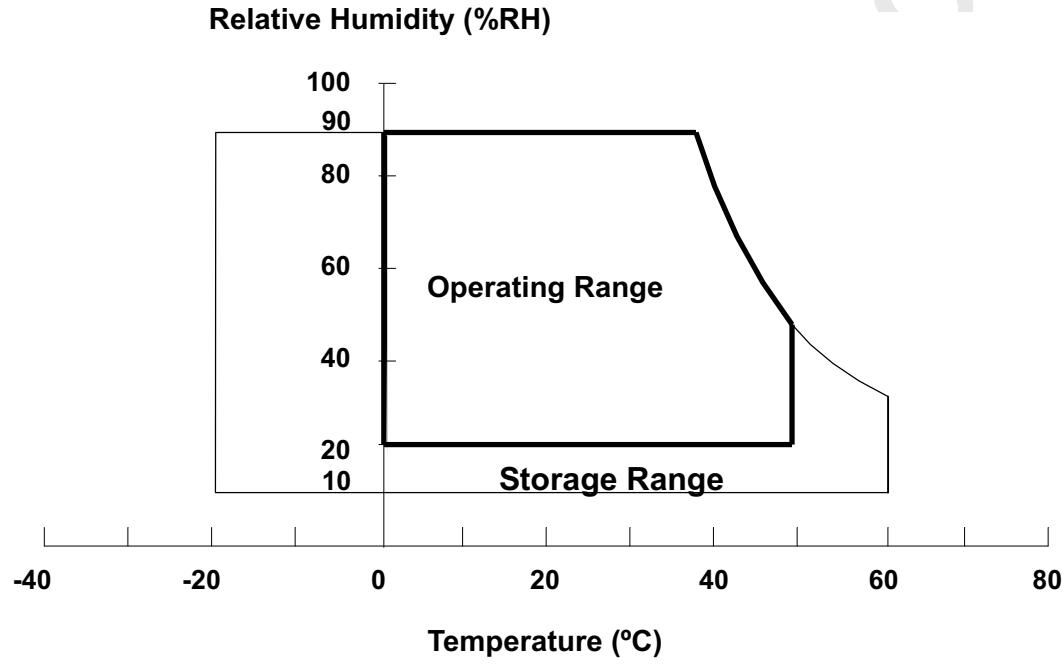
### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	$T_{ST}$	-20	60	°C	(1)
Operating Ambient Temperature	$T_{OP}$	0	50	°C	(1), (2)
Shock (Non-Operating)	$S_{NOP}$	-	50	G	(3), (5)
Vibration (Non-Operating)	$V_{NOP}$	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ( $T_a \leq 40$  °C).
- (b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40$  °C).
- (c) No condensation.

Note (2) The temperature of panel display surface area should be 0 °C Min. and 60 °C Max.

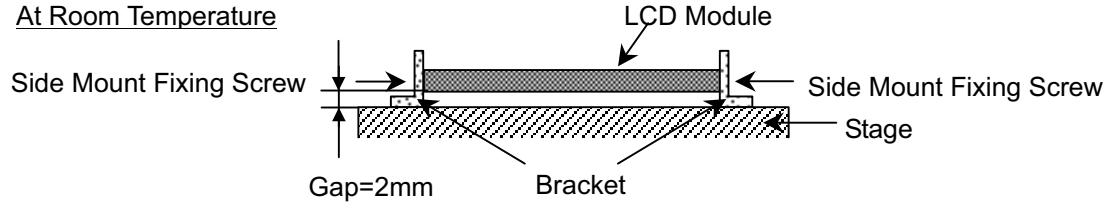


Note (3) 50G 11ms, half sine wave, 1 time for  $\pm X$ ,  $\pm Y$ ,  $\pm Z$ .

Note (4) 10 ~ 300 Hz, 10min/cycle, 3 cycles each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:





## 2.2 ELECTRICAL ABSOLUTE RATINGS

### 2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V <sub>cc</sub>	-0.3	+6.0	V	
Logic Input Voltage	V <sub>IN</sub>	-0.3	4.3	V	(1)

### 2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V <sub>L</sub>	-	2.5K	V <sub>RMS</sub>	(1), (2), I <sub>L</sub> = 7.0mA
Lamp Current	I <sub>L</sub>	-	7.5	mA <sub>RMS</sub>	
Lamp Frequency	F <sub>L</sub>	-	80	KHz	(1), (2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).



### 3. ELECTRICAL CHARACTERISTICS

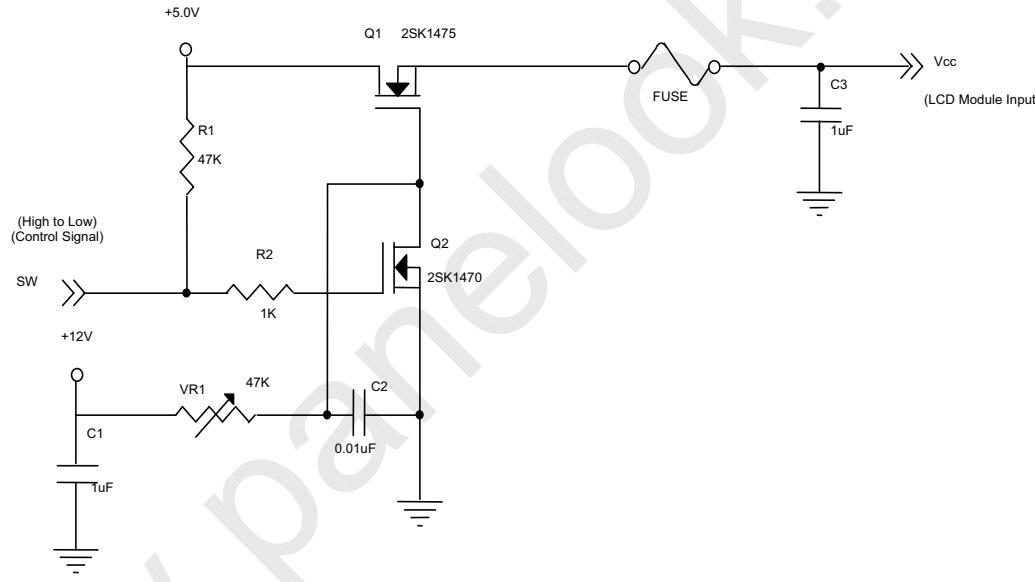
#### 3.1 TFT LCD MODULE

$T_a = 25 \pm 2 ^\circ C$

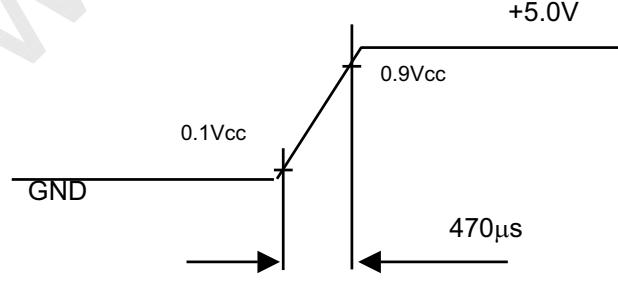
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	-
Ripple Voltage	V <sub>RP</sub>	-	-	100	mV	-
Rush Current	I <sub>RUSH</sub>	-	2	3	A	(2)
Power Supply Current	White	-	0.5	0.8	A	(3)a
	Black	-	1.3	1.5	A	(3)b
	Vertical Stripe	-	0.9	1.3	A	(3)c
LVDS differential input voltage	V <sub>id</sub>	100	-	600	mV	
LVDS common input voltage	V <sub>ic</sub>	-	1.2	-	V	
Logic "L" input voltage	V <sub>il</sub>	V <sub>ss</sub>	-	0.8	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



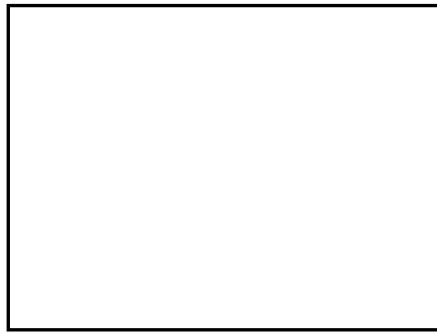
Vcc rising time is 470μs





Note (3) The specified power supply current is under the conditions at  $V_{cc} = 5.0$  V,  $T_a = 25 \pm 2$  °C,  $f_v = 60$  Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



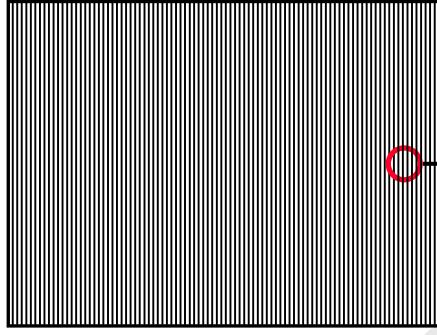
Active Area

b. Black Pattern

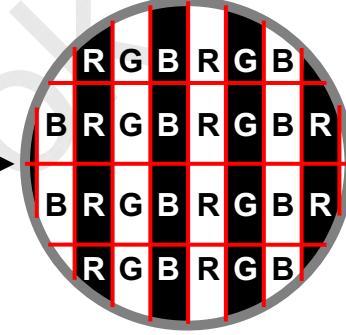


Active Area

c. Vertical Stripe Pattern



Active Area



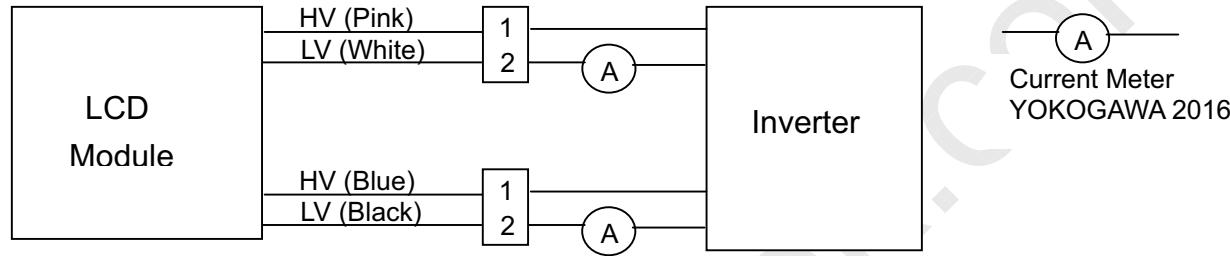


## 3.2 BACKLIGHT UNIT

 $T_a = 25 \pm 2 ^\circ C$ 

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	$V_L$	605	670	735	$V_{RMS}$	$I_L = 7 \text{ mA}$
Lamp Current	$I_L$	2.0	7.0	7.5	$\text{mA}_{RMS}$	(1)
Lamp Turn On Voltage	$V_S$	---	---	1650 ( $0^\circ C$ )	$V_{RMS}$	
		---	---	1185 ( $25^\circ C$ )	$V_{RMS}$	(2)
Operating Frequency	$F_L$	40	---	80	KHz	(3)
Lamp Life Time	$L_{BL}$	40000	---	---	Hrs	(5)
Power Consumption	$P_L$	---	18.76	---	W	(4), $I_L = 7 \text{ mA}$

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup.

Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4)  $P_L = I_L \times V_L \times 4 \text{ CCFLs}$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition

$T_a = 25 \pm 2 ^\circ C$  and  $I_L = 7.0 \text{ mA}_{RMS}$  until one of the following events occurs:

- (a) When the brightness becomes or lower than 50% of its original value.
- (b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

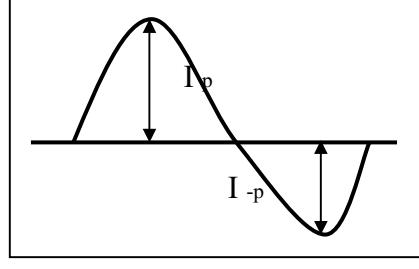
Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.



The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- a. The asymmetry rate of the inverter waveform should be 10% below;
- b. The distortion rate of the waveform should be within  $\sqrt{2} \pm 10\%$ ;
- c. The ideal sine wave form shall be symmetric in positive and negative polarities.



\* Asymmetry rate:

$$| I_p - I_{-p} | / I_{rms} * 100\%$$

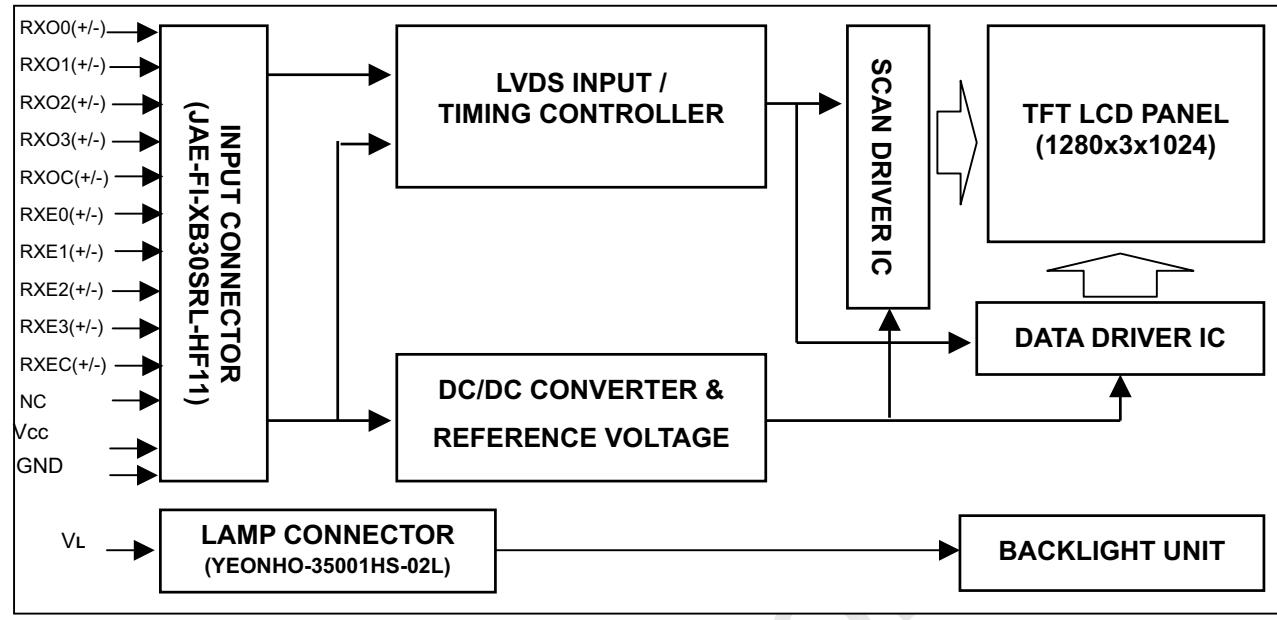
\* Distortion rate

$$I_p (\text{or } I_{-p}) / I_{rms}$$

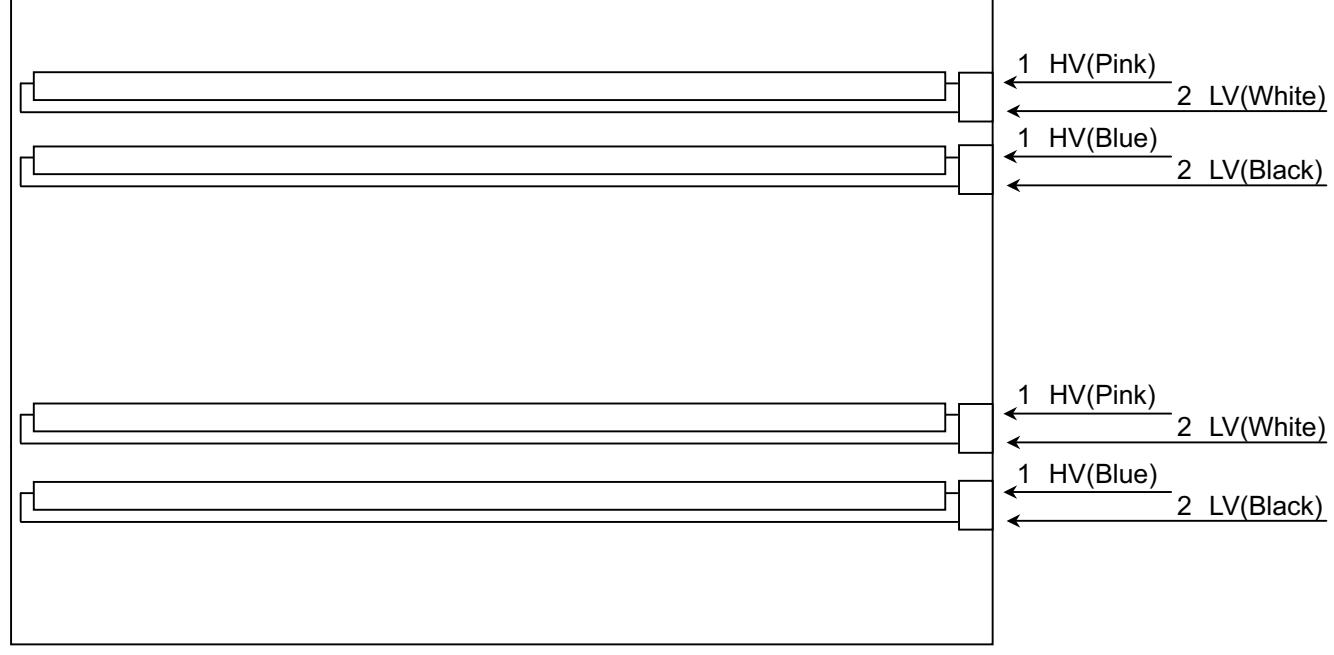


## 4. BLOCK DIAGRAM

### 4.1 TFT LCD MODULE



### 4.2 BACKLIGHT UNIT





## 5. INPUT TERMINAL PIN ASSIGNMENT

### 5.1 TFT LCD MODULE

1	RX00-	Negative LVDS differential data input. Channel O0 (odd)
2	RX00+	Positive LVDS differential data input. Channel O0 (odd)
3	RX01-	Negative LVDS differential data input. Channel O1 (odd)
4	RX01+	Positive LVDS differential data input. Channel O1 (odd)
5	RX02-	Negative LVDS differential data input. Channel O2 (odd)
6	RX02+	Positive LVDS differential data input. Channel O2 (odd)
7	GND	Ground
8	RXOC-	Negative LVDS differential clock input. (odd)
9	RXOC+	Positive LVDS differential clock input. (odd)
10	RXO3-	Negative LVDS differential data input. Channel O3(odd)
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXE0-	Negative LVDS differential data input. Channel E0 (even)
13	RXE0+	Positive LVDS differential data input. Channel E0 (even)
14	GND	Ground
15	RXE1-	Negative LVDS differential data input. Channel E1 (even)
16	RXE1+	Positive LVDS differential data input. Channel E1 (even)
17	GND	Ground
18	RXE2-	Negative LVDS differential data input. Channel E2 (even)
19	RXE2+	Positive LVDS differential data input. Channel E2 (even)
20	RXEC-	Negative LVDS differential clock input. (even)
21	RXEC+	Positive LVDS differential clock input. (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXE3+	Positive LVDS differential data input. Channel E3 (even)
24	GND	Ground
25	TEST	Test pin should be tied to ground.
26	NC	Not connection.
27	NC	Not connection.
28	VCC	+5.0V power supply
29	VCC	+5.0V power supply
30	VCC	+5.0V power supply

Note (1) Connector Part No.: JAE-FI-XB30SRL-HF11 or equivalent.

Note (2) The first pixel is odd.

Note (3) Input signal of even and odd clock should be the same timing.



LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6



## 5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Remark
1	HV	High Voltage	Pink
2	LV	Low Voltage	White
1	HV	High Voltage	Blue
2	LV	Low Voltage	Black

Note (1) Connector Part No.: 35001HS-02 (YEONHO) or equivalent

Note (2) User's connector Part No.:SM02B-BHSS-1-TB (JST) or equivalent

## 5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red(253)	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green(253)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage



## 6. INTERFACE TIMING

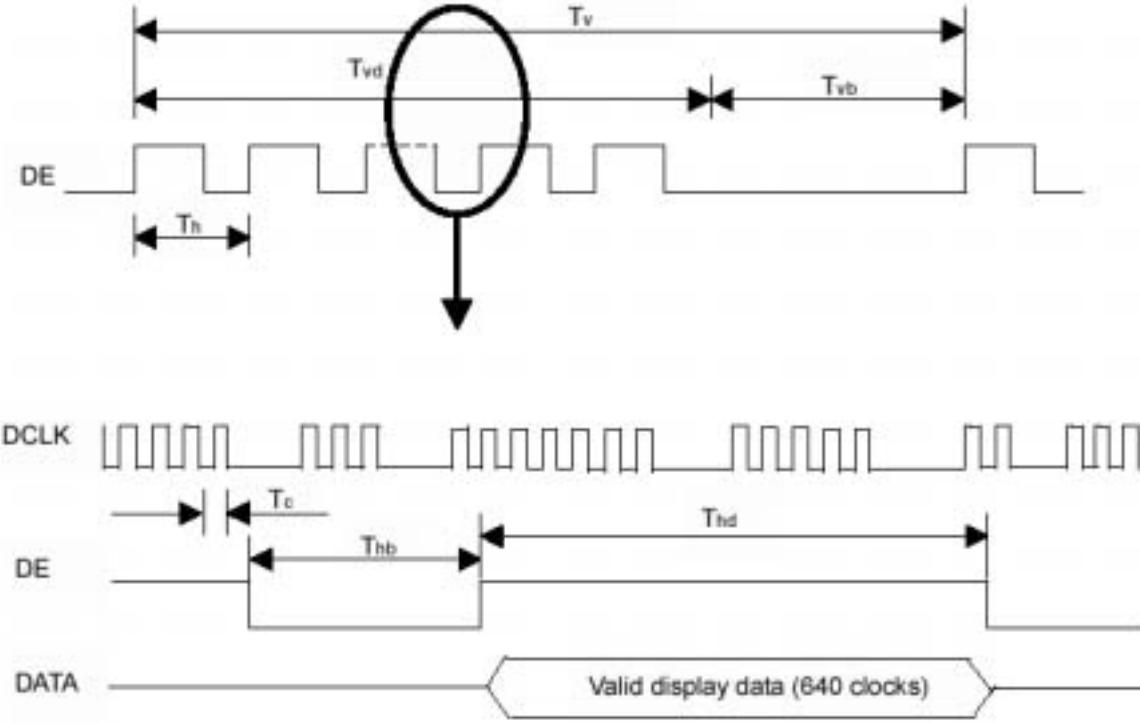
### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F <sub>c</sub>	-	54	67.5	MHz	-
	Period	T <sub>c</sub>	-	18.5	-	ns	
	High Time	T <sub>ch</sub>	-	4/7	-	T <sub>c</sub>	-
	Low Time	T <sub>cl</sub>	-	3/7	-	T <sub>c</sub>	-
LVDS Data	Setup Time	T <sub>lvs</sub>	600	-	-	ps	-
	Hold Time	T <sub>lvh</sub>	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	F <sub>r</sub>	56	60	75	Hz	T <sub>v</sub> =T <sub>v</sub> d+T <sub>v</sub> b
	Total	T <sub>v</sub>	1034	1066	1274	Th	-
	Display	T <sub>v</sub> d	1024	1024	1024	Th	-
Horizontal Active Display Term	Blank	T <sub>v</sub> b	10	42	T <sub>v</sub> -T <sub>v</sub> d	Th	-
	Total	T <sub>h</sub>	740	844	960	T <sub>c</sub>	T <sub>h</sub> =T <sub>hd</sub> +T <sub>hb</sub>
	Display	T <sub>hd</sub>	640	640	640	T <sub>c</sub>	-
	Blank	T <sub>hb</sub>	100	204	T <sub>h</sub> -T <sub>hd</sub>	T <sub>c</sub>	-

Note: Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

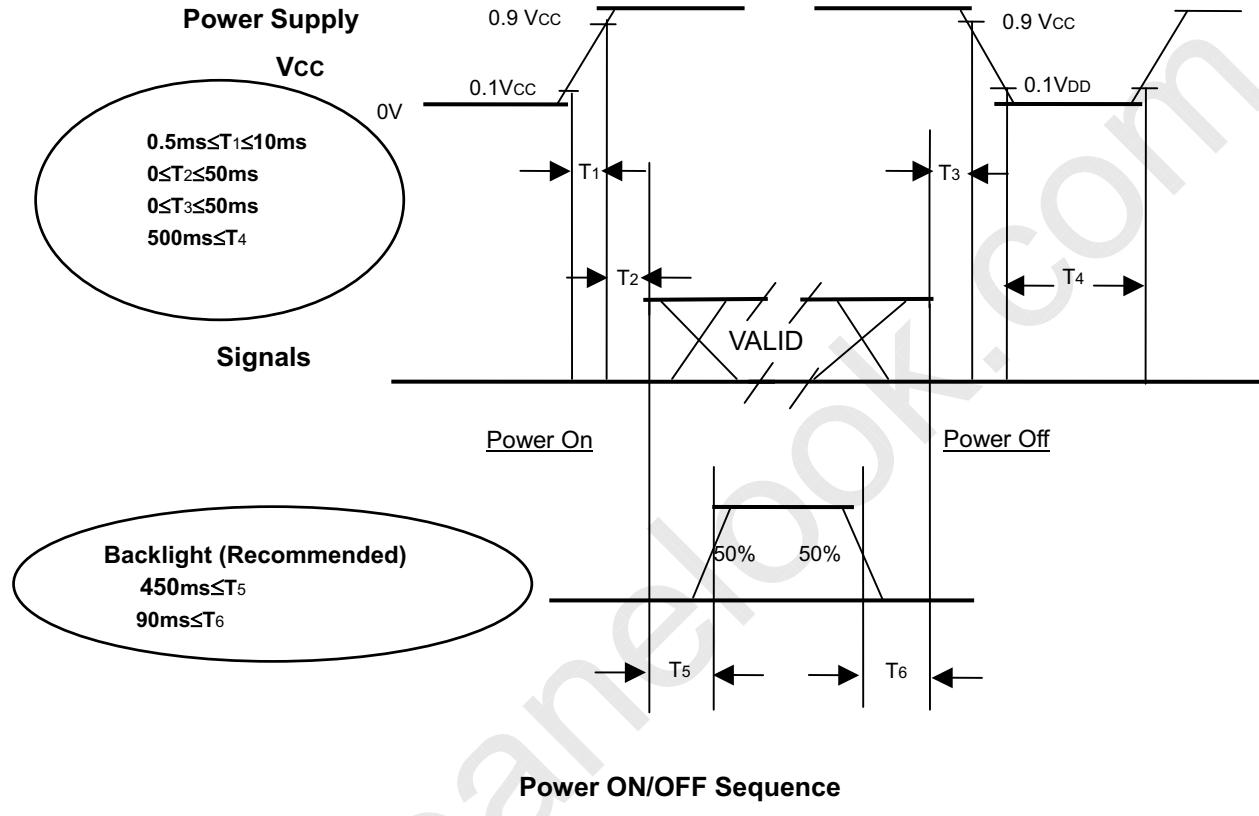
### INPUT SIGNAL TIMING DIAGRAM





## 6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note.

- (1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.
- (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.



Issued Date: May. 30, 2007  
Model No.: M190E5-L0E

Approval

## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

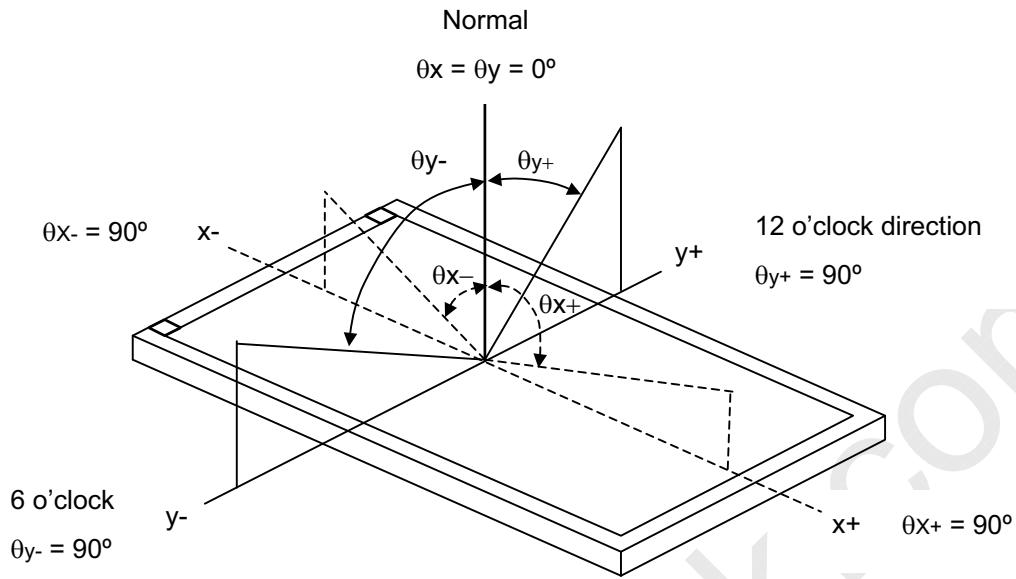
Item	Symbol	Value	Unit
Ambient Temperature	T <sub>a</sub>	25±2	°C
Ambient Humidity	H <sub>a</sub>	50±10	%RH
Supply Voltage	V <sub>CC</sub>	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I <sub>L</sub>	7	mA
Inverter Operating Frequency	F <sub>L</sub>	61	KHz
Inverter	SUMIDA H05 5307		

### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note		
Color Chromaticity	Red	$\theta_x=0^\circ, \theta_Y=0^\circ$ CS-1000T	Typ - 0.03	0.645	Typ + 0.03	(1), (6)			
				0.332					
	Green			0.285					
				0.600					
	Blue			0.151					
				0.074					
	White			0.313					
				0.329					
Center Luminance of White	L <sub>c</sub>		250	300	---	cd/m <sup>2</sup>	(4), (6)		
Contrast Ratio	CR		450	800	---	-	(2), (6)		
Response Time	T <sub>R</sub>	$\theta_x=0^\circ, \theta_Y=0^\circ$	---	1.3	6	ms	(3)		
	T <sub>F</sub>			3.7					
White Variation	δW	$\theta_x=0^\circ, \theta_Y=0^\circ$ BM-5A	1.25	1.33	---	-	(6), (7)		
Viewing Angle	Horizontal	$CR \geq 10$ BM-5A	75	85	---	Deg.	(1), (6)		
			75	85	---				
	Vertical		70	80	---				
			70	80	---				

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

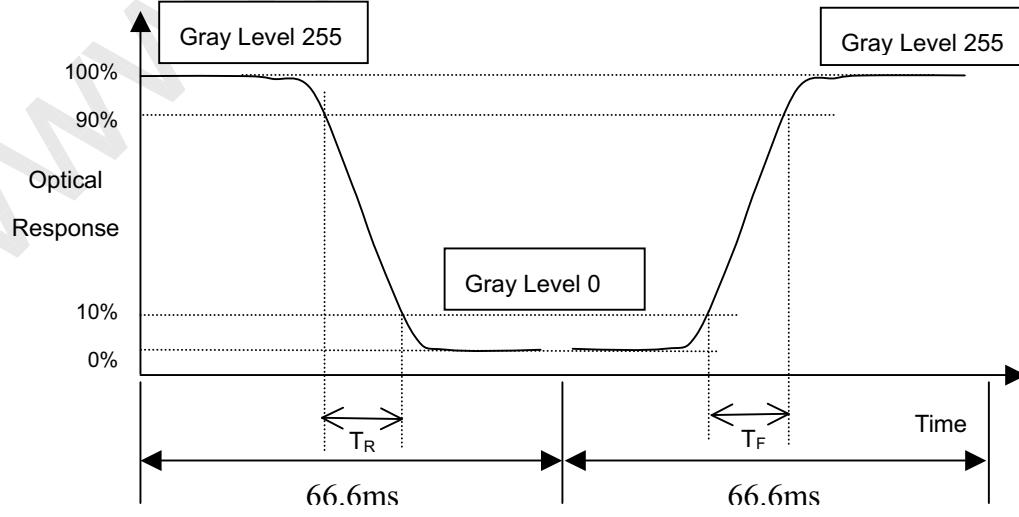
L255: Luminance of gray level 255

L0: Luminance of gray level 0

$$CR = CR(5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (3) Definition of Response Time ( $T_R, T_F$ ):



Note (4) Definition of Luminance of White ( $L_C$ ):

Measure the luminance of gray level 255 at center point

$$L_C = L(5)$$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (7).

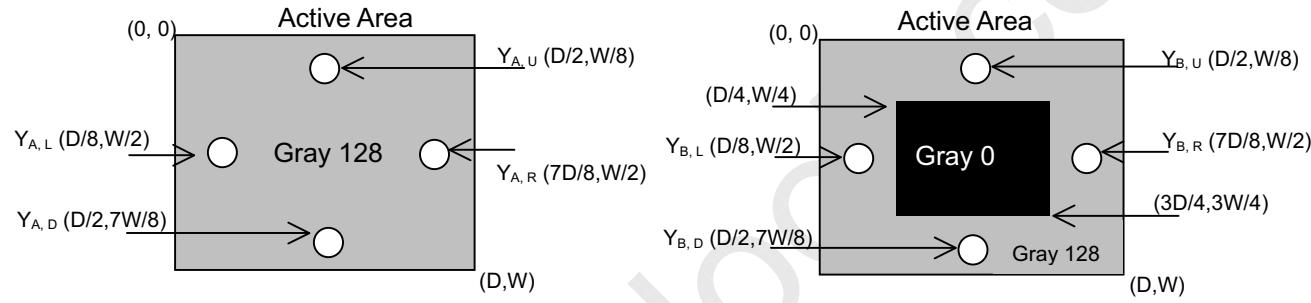
## Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

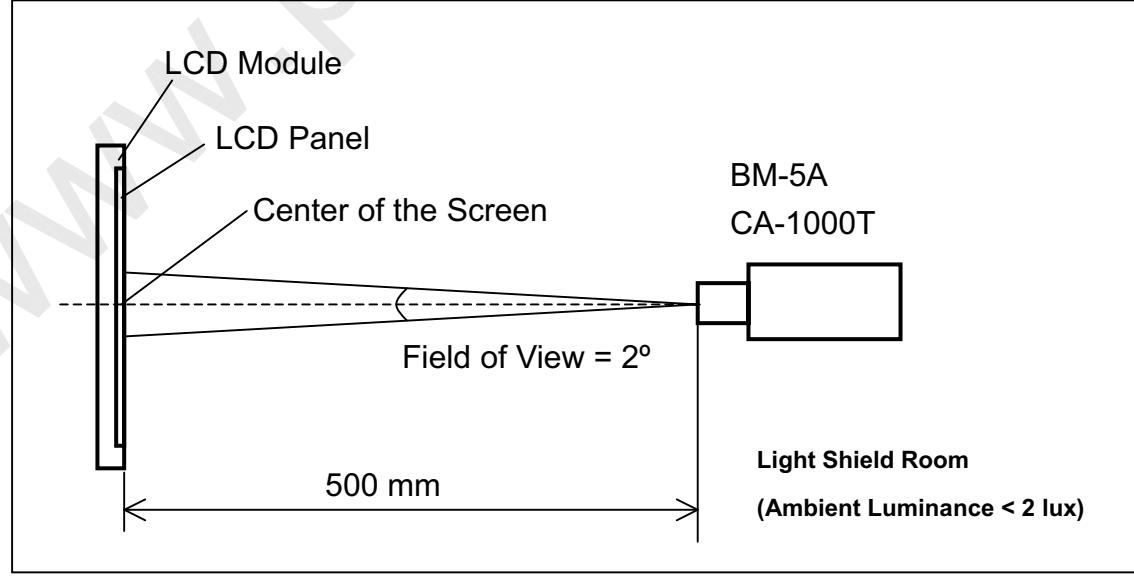
$Y_A$  = Luminance of measured location without gray level 0 pattern ( $cd/m^2$ )

$Y_B$  = Luminance of measured location with gray level 0 pattern ( $cd/m^2$ )



## Note (6) Measurement Setup:

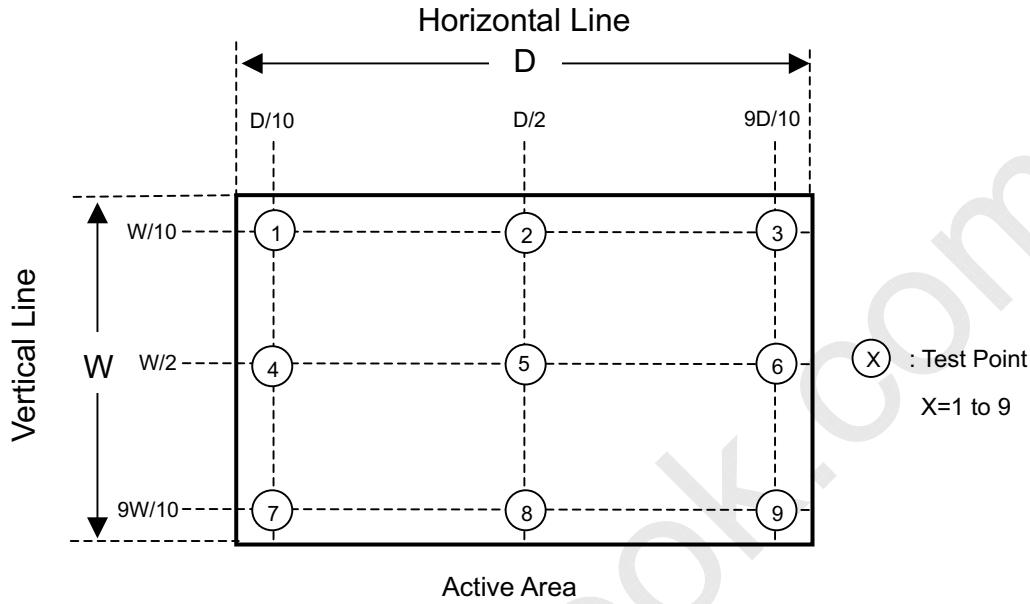
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (7) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 255 at 9 points

$$\delta W = \text{Maximum} [L(1), L(2), \dots, L(4), L(9)] / \text{Minimum} [L(1), L(2), \dots, L(4), L(9)]$$



Note (8) Definition of Gamma Value ( $\gamma$ )

According to VESA FPDM Version 2.0 section "302-5A"

$$L = a * G^\gamma + L_b$$

$$\log(L - L_b) = \gamma * \log(G) + \log(a)$$

L : Luminance

a : Constant

G : Gray level

$L_b$  : Luminance at dark state

$\gamma$  is the slope that best fits the  $\log(L - L_b) - \log(G)$  data.

Gray level is "0,16,32,48,64,96,128.....255"



## 8. PACKAGING

### 8.1 PACKING SPECIFICATIONS

- (1) 5 LCD modules / 1 Box
- (2) Box dimensions: 537(L) X 316(W) X 462(H) mm
- (3) Weight: approximately 11Kg (5 modules per box)

### 8.2 PACKING METHOD

- (1) Carton Packing should have no failure in the following reliability test items.

Test Item	Test Conditions	Note
Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Dropping Test	1 Angle, 3 Edge, 6 Face, 60cm	Non Operation

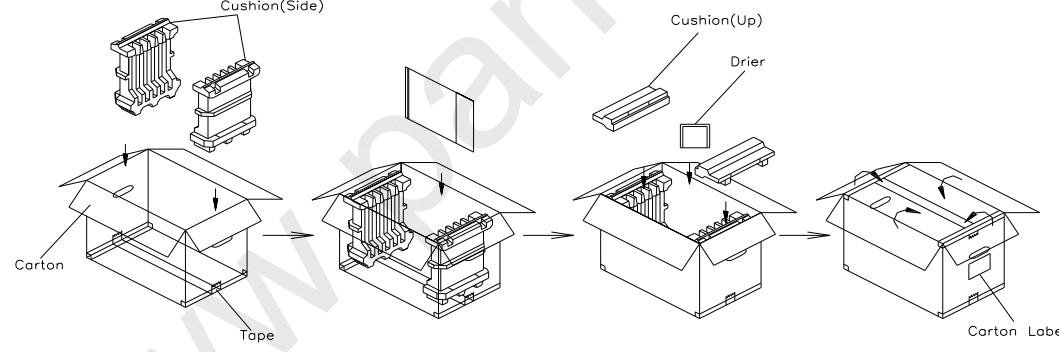
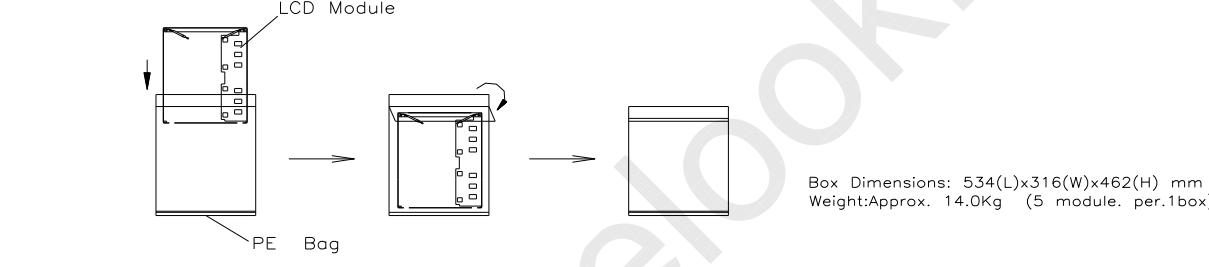
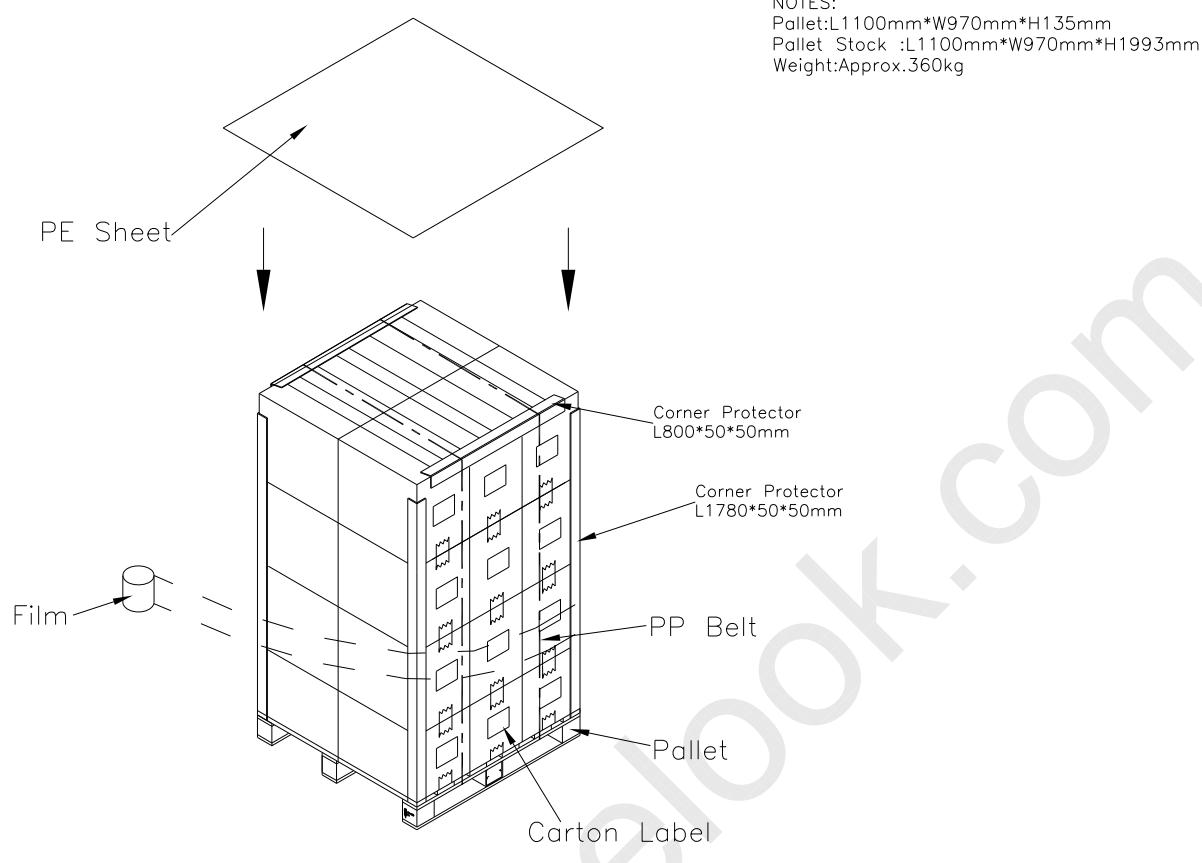


Figure. 8-1 Packing method

**Figure. 8-2 Packing method**



## 9. DEFINITION OF LABELS

### 9.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: M190E5-L0E
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U.
L	Product line #	Line 1=1, Line 2=2, Line 3=3, ...
NNNN	Serial number	Manufacturing sequence of product

- (d) Customer's barcode definition:

Serial ID: CM-19E5E-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
19E5E	Model number	M190E5-L0E=19E5E
X	Revision code	ZBD Grade: A~J ; Non ZBD Grade:1~9
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN ; Ningbo, China =NP
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, T, U, V
NNNN	Serial number	By LCD supplier



## 10. PRECAUTIONS

### 10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

### 10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

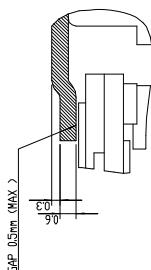
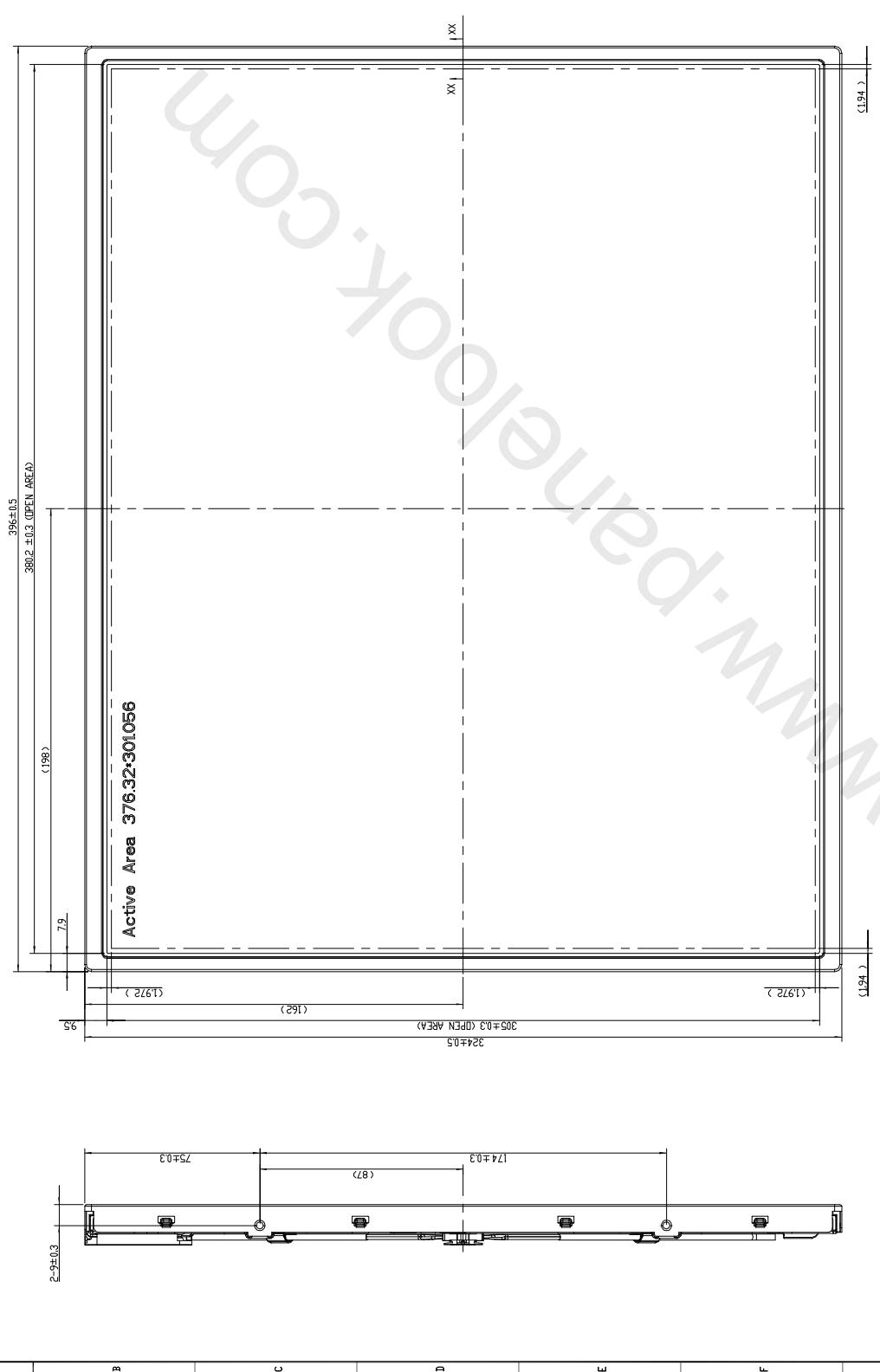
14076097



屏库: 全球液晶屏交易中心

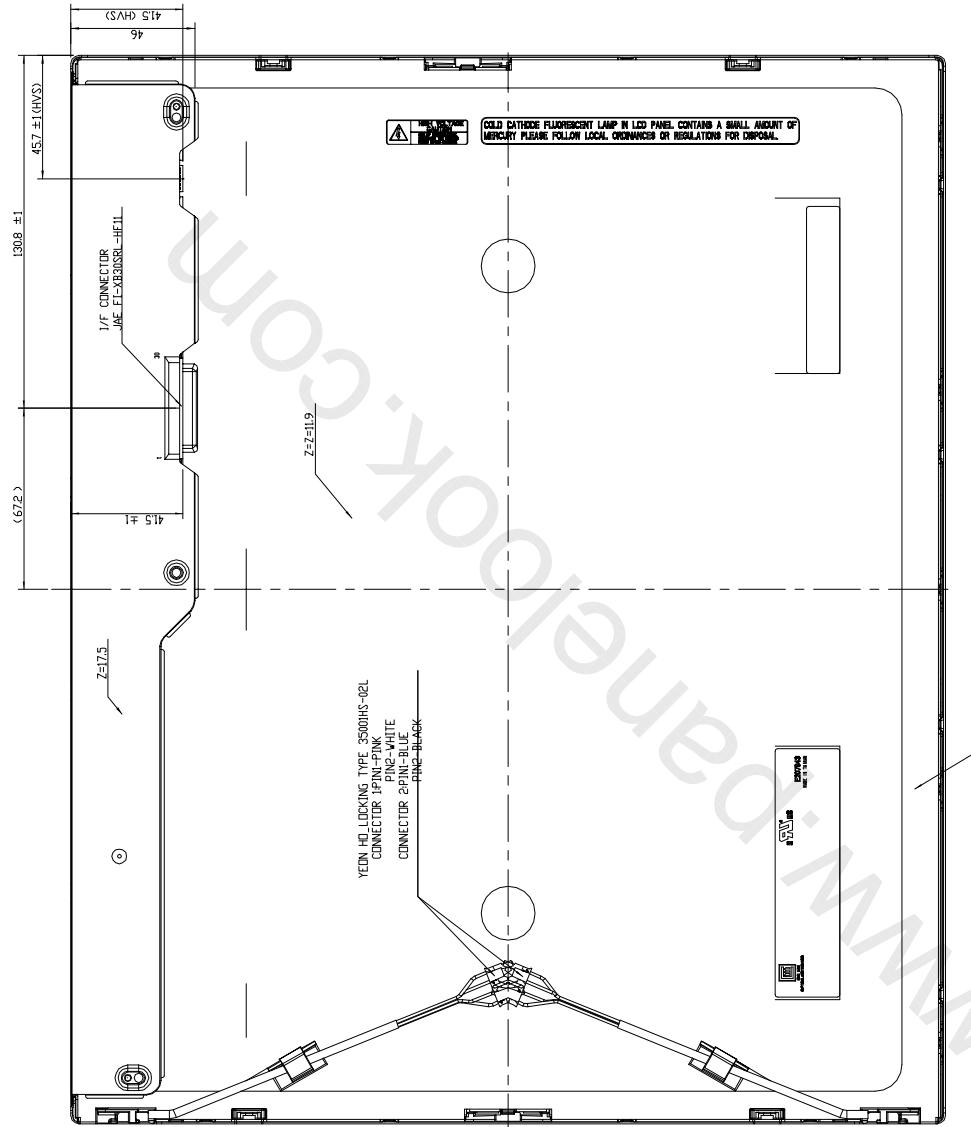
www.panelook.com

Global LCD Panel Exchange Center

SECTION XX-XX  
SCALE 10:1

NOTE:  
1.DUFLINE TOLERANCE ±0.5mm  
2.17P CONNECTOR SPECIALE F1-XB30SRL-H#11  
3.LAMP CONNECTOR(FIN) LOCKING TYPE: SG90US-02L  
4.SIDE MOUNT HOLE ROTATION TORQUE MUST BE MAX.5kgf-cm

TITLE: ASSY MODULE MMPS5-LUE903		REV.: A
Approved	TECH. CHNG	Drawing No.
Checked	TO BASE WANG	M8207424H
Drawn	AMINA PAN	Part No.
Designer	TO BASE WANG	TSB
Date: 2016-02-26		Sheet 1 / 2 Al
Base: 2016-02-26 Scale: N Unitem		CHI MEI
ALL RIGHTS RESERVED, © CHI MEI DISPLAY ELECTRONICS CORP.		



NOTE:  
 1.DUFLINE TOLERANCE<±0.2mm  
 2.1/F CONNECTOR SPEC:JAE F-XB30SRL-HF11  
 3.LAMP CONNECTOR(ON TO LOCKING) TYPE 3500HS-02L  
 4.SSIDE MOUNT HOLE ROTATION TORQUE MUST BE MAX 3.5kg·cm

TITLE: ASSY MODULE MMPS5-LUE903		REV: A
Approved	TEK CHENG	Drawing No. M827424A
Checked	TOBIAO WANG	Part No. TB
Drawer	ADINA PAN	Material No.
Designer	TOBIAO WANG	Date 15-Mar-2007 Scale 1:1 Unit mm
[CH] MET		ALL RIGHTS RESERVED, OWNERSHIP RESERVED. DEUTSCH ELECTRONICS CORP.